Design of GaN X-band Two-Stage Doherty Power Amplifier

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***Abstract*— A thermal imaging technique is used to characterize an X-band two-stage Doherty power amplifier (DPA) design that used QFN packaged discrete GaN devices. The technique can be used to optimize the Doherty amplifier operation at the intended back-off output power point to meet linearity requirements with optimum efficiency across the band. The temperature difference between the four discrete devices of the two-stage Doherty design shows when the peaking branch of the amplifier kicks in to assist the carrier branch power operation, which can be adjusted by tuning the cut-off voltage bias of the two-stage Peak devices. The implemented DPA exhibited a maximum gain of 18 dB and an output power of 46 dBm over the frequency range from 8.0 to 8.5 GHz, with a maximum efficiency of 30% at a 6 dB back-off output power level of 40 dBm. The experimentally observed results match with the results of large signal simulation and can be used to optimize the Doherty amplifier design to meet system requirements.**

***Keywords*— Doherty, GaN, Power Amplifier, X-Band.**

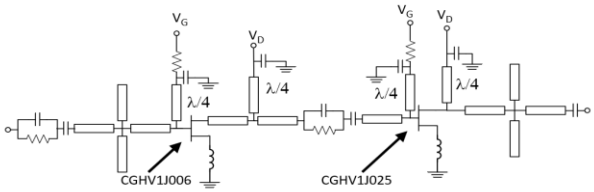
I. Introduction

Gallium-Nitride High Electron Mobility Transistors (GaN-HEMT) have been used in Doherty Power Amplifier (DPA) designs at X-band to obtain high efficiency at 6 dB back-off operation; see for example [1] where a two-stage implementation of the DPA was carried out using CREE bare die devices with harmonic tuning done at the chip level with bond-wires and capacitors. The DPA requires two parallel amplifiers which are the carrier amplifier and the peaking amplifier. Efficiency of at an output power back-off can be improved by load impedance modulation using a quarter-wave impedance transformer at the load network [2-6].

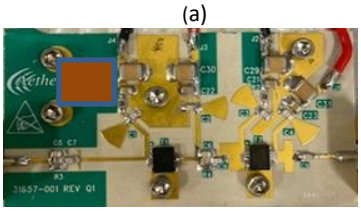
In this paper we present a two-stage DPA design using QFN packaged CREE devices to meet a system Noise Power Ratio (NPR) specification of 14.5 dB which required the amplifier to operate with good efficiency at about 6-dB back-off from its 50 W saturated output power. The design was optimized with large signal simulation of the DPA using device non-linear models of the CREE devices. A CREE CGHV1F006S (6 W) GaN HEMT packaged device was used to drive a CGHV1F025S (25 W) GaN HEMT packaged device also from CREE. The input, output and intermediate matching circuits were designed and optimized using harmonic balance simulation of the circuit utilizing non-linear models of the devices.

II. Design of two-stage PA

A schematic of the X-band two-stage PA using the packaged GaN-HEMTS is shown in Fig. 1a. Input matching, inter-stage matching, and load matching networks were implemented on a printed circuit board (PCB) of 10 mil thickness and with 18 plated vias under each packaged device. The plated vias can be replaced with a copper-coined PCB implementation for better thermal operation under CW conditions.



(a)



(b)

Figure 1. (a) Schematic of designed GaN-HEMT single-ended two-stage PA. (b) Implemented two-stage PA design.

The parallel R and C networks, at the input and inter-stage in the schematic, are necessary for stability of the amplifier. The plated via inductance, under each of the two devices, was represented by a parasitic inductance as shown in Fig 1a. Quarter-wave lines are used to supply biases. Electromagnetic simulation was performed on the laid-out amplifier using Sonnet software to validate the harmonic balance simulation. Fig. 1b shows the implemented two-stage PA.

The small signal measured performance of the two-stage PA showed excellent agreement with harmonic balance simulation and Sonnet electromagnetic simulation as is seen in Fig. 2. The board was also tested for large signal operation and the testing was done for pulsed operation with a pulse width of 10 ms and duty cycle of 20%. The result of the power testing is shown in Fig. 3a and compared to the harmonic balance simulation in Fig. 3b and is seen to have very good agreement as well. An efficiency of 35% was obtained at about 41 dBm with gain of 22.5 dB.

The testing of the single-ended two-stage PA was crucial to the design and build of the two-stage DPA which used the

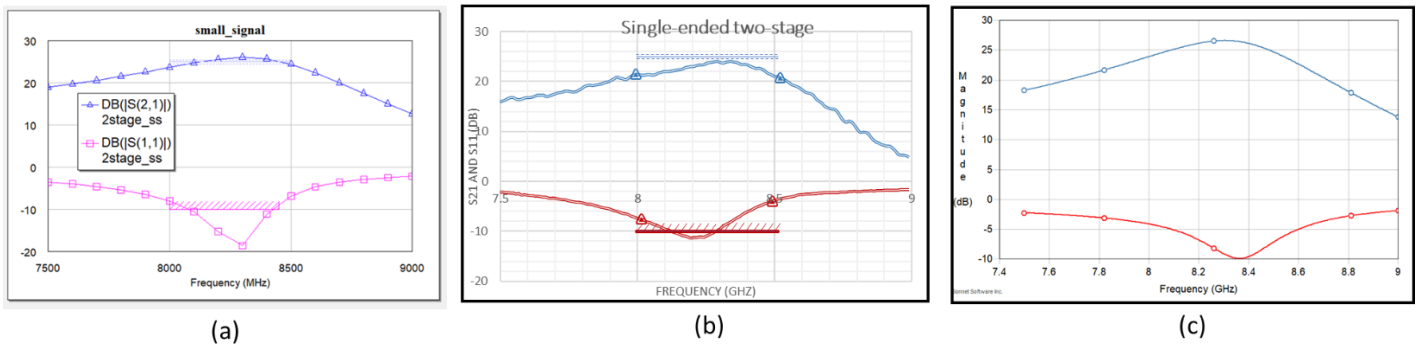


Figure 2. Measurement and simulation of the single-ended two stage PA. (a) Microwave Office simulation. (b) Measurement. (c) Sonnet EM simulation.

same two-stage amplifier in both carrier and peaking arms as will be described in the next section.

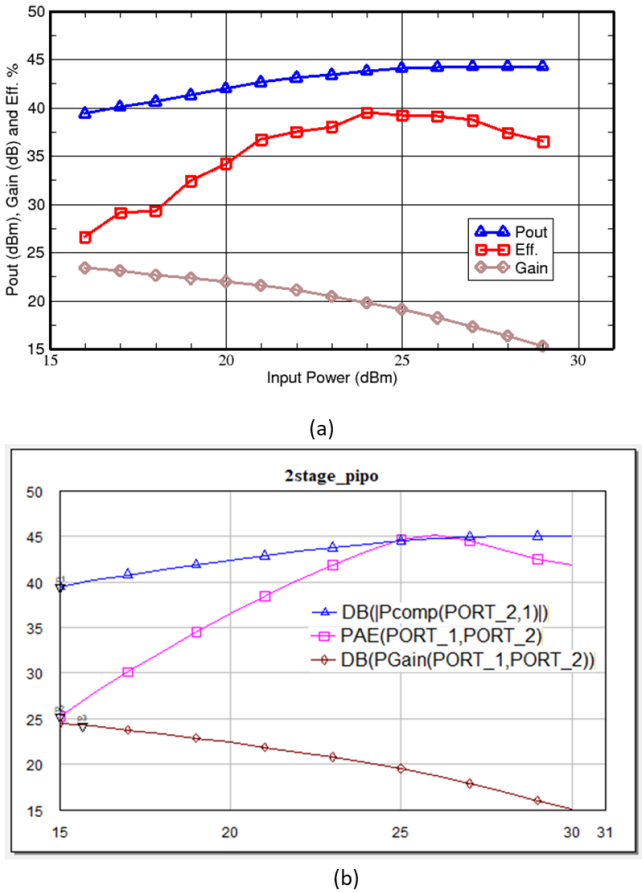


Figure 3. Measured and simulated power, efficiency and gain at 8.3 GHz of the single-ended two-stage power amplifier. (a) Pulsed measurement with 10 ms pulse and 20% duty cycle. (b) Harmonic balance simulation.

III. Two-Stage Doherty PA

The block diagram of the GaN-HEMT two-stage DPA is shown in Fig. 4a. Two two-stage PAs were used as the Carrier and Peaking PAs. The input signal is split using a Wilkinson power divider. Load impedance modulation is obtained by using a quarter-wave transmission line after the carrier PA.

The optimized offset lines after the load matching networks of the Carrier and Peaking PAs allow a proper load impedance modulation and maximum efficiency enhancement for the DPA. The drive and main stages for the carrier PA have Class-AB operation, while the drive and main stages for the peaking PA have Class-B and Class-C operations, respectively, with both biases optimized using thermal imaging technique as will be discussed in the next section.

The implemented two-stage DPA board is shown in Fig. 4b and is based on the single-ended two-stage PA described earlier.

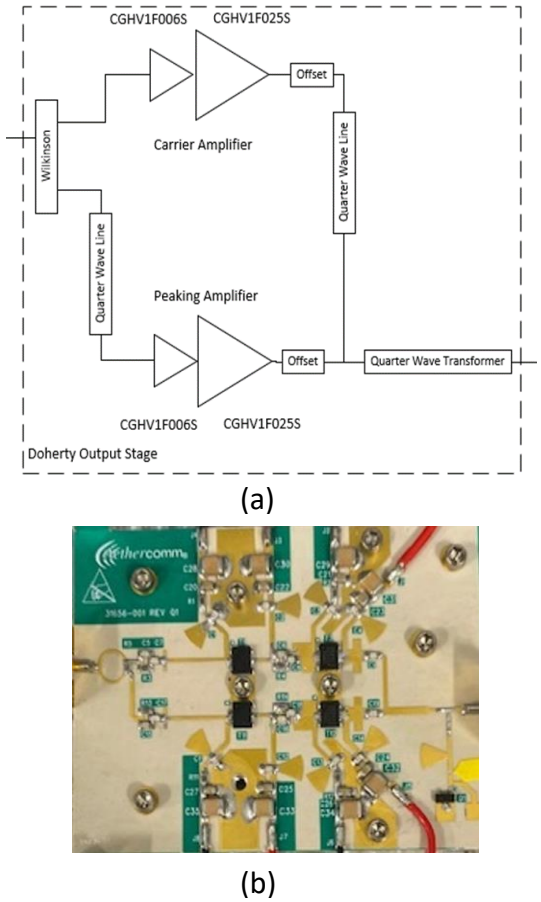


Figure 4. (a) Two-stage DPA block diagram. (b) Implemented two-stage DPA.

The small signal performance of the two-stage DPA is shown in Fig. 5. It shows a gain of 21 dB across the intended band of 8 to 8.5 GHz, which was measured with the carrier devices biased at 40 V and -2.7 V, and the peaking devices biased at 40V and -5 V.

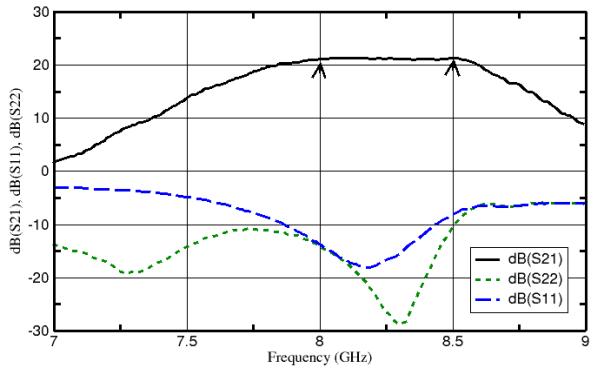
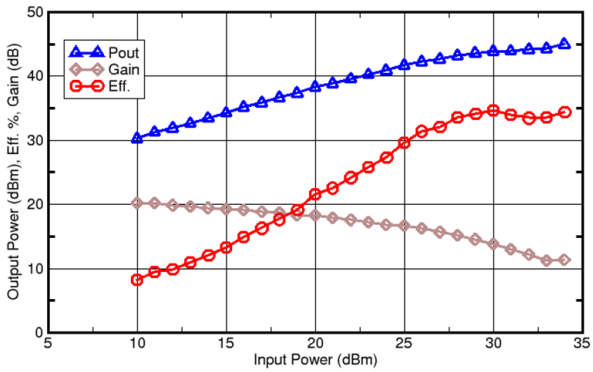
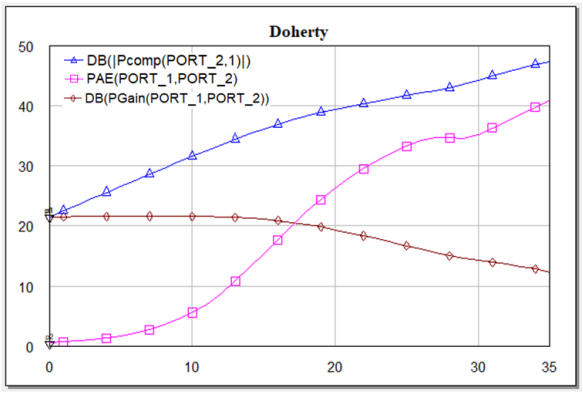


Figure 5. Two-stage DPA small signal gain measurement. Carrier devices at 40 V and -2.7 V, and peaking devices at 40 V and -5 V.

The power measurement at 8.2 GHz is shown in Fig. 6a below and compared to the simulated two-stage DPA simulation to show that good agreement was obtained between them.



(a)



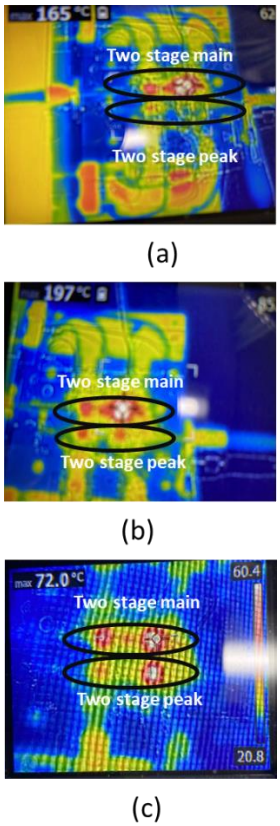
(b)

Figure 6. (a) Two-stage DPA power measurement. (b) Harmonic balance simulation.

The intended nominal operating point of operation is at about 40.7 dBm which is at 6 dB output back-off. At that point the efficiency is about 30% and the gain is about 17 dB. The operation of the DPA was optimized by tuning the devices bias which controlled when the peaking amplifier branch started to assist the carrier branch using thermal imaging technique as will be shown in the next section.

IV. Thermal Imaging Optimization of DPA

The point at which the Peaking amplifier starts assisting the Carrier amplifier is crucial in optimizing the operation of the DPA in order to obtain maximum efficiency at the desired back-off point. This is best done with thermal imaging technique that shows when the peaking amplifier devices start to kick in, which could be adjusted by tweaking their biases. Fig. 7a shows that at an output power of 39 dBm, the first stage of the peaking amplifier was about to turn on while the second stage was still off. Fig. 7b is the thermal image taken at output power of 40.6 dB, and shows that now both peaking devices are turned on. Fig. 7c is the thermal image at output power of 45 dBm and shows that the second stage device now is almost at full power and equally contributing to the output power of the DPA near saturation.



(a)

(b)

(c)

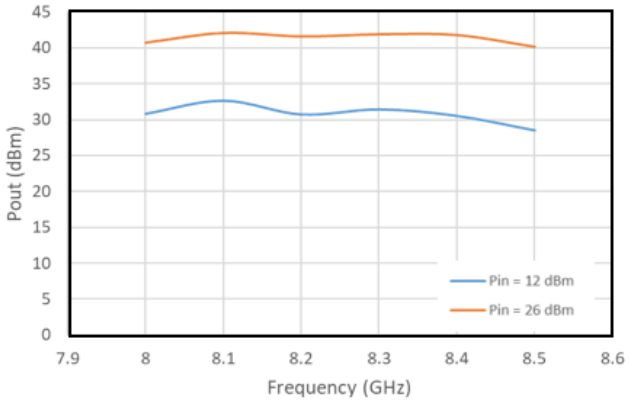
Figure 7. Thermal images of the two-stage DPA in operation. (a) At output power of 39 dBm. (b) At output power of 40.6 dBm. (c) At output power of 45 dBm.

The optimized offset lines, after the load matching networks of the carrier and peaking Pas, allow a proper load impedance modulation and maximum efficiency enhancement for the DPA, which, in addition to the bias tuning described above, could achieve the desired performance of the DPA at the 6-dB back off condition with best efficiency across the band.

V. Power Measurements on the Optimized DPA

The design goal of this two-stage DPA was to have maximum efficiency at an output power of 40 dBm after taking into account the output network losses. The thermal imaging bias tuning described in the previous section was utilized to achieve this goal, and the measurements shown in Fig. 8 demonstrate that the design goal was fulfilled across the DPA bandwidth from 8 to 8.4 GHz where optimum efficiency was achieved at the intended nominal operating point of about 41 dBm across the band.

As can be seen an efficiency of 23 to 30% was obtained from 8 to 8.4 GHz at the 6-dB output back-off condition.



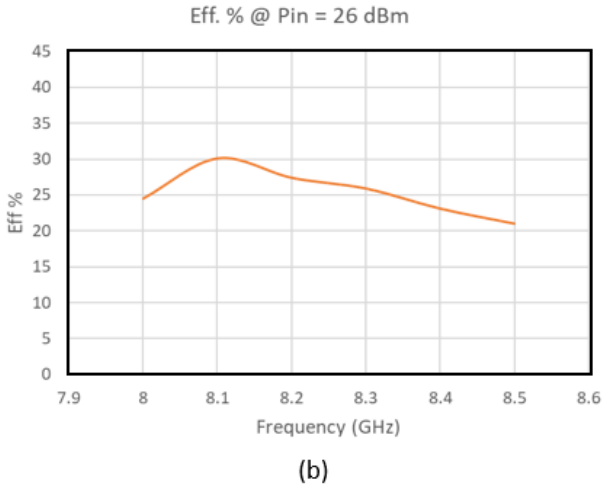


Figure 8. Output power and efficiency measurement across the band. (a) Output power at input power of 12 dBm and 26 dBm. (b) Efficiency at input power of 26 dBm resulting in about 41 dBm across the band.

The results across the band, shown in Fig. 8, demonstrate the DPA performance at 30 dBm and 40 dBm power levels between 8 and 8.4 GHz after taking into account the output network loss. A maximum efficiency of 30% was obtained at 6 dB output back-off. Overall, the efficiency at 6-dB back-off was between 23 and 30% over the band from 8 to 8.4 GHz.

VI. Conclusion

In this paper a two-stage DPA was designed and implemented using discrete QFN packaged GaN-HEMT devices. The implemented DPA exhibited a maximum gain of 18 dB, and output of about 46 dBm in the band from 8 to 8.5 GHz. An optimum efficiency of about 30% was obtained within the design band that was optimized to be maximum at the 6-dB output power back-off operation point.

The optimization, of the optimum efficiency of the DPA, was achieved using experimental bias tuning of the peaking devices as observed from their turn-on point viewed from thermal imaging of the DPA. The temperature difference between the four discrete devices of the two-stage Doherty design shows when the peaking branch of the amplifier kicks in to assist the carrier branch power operation, which could be adjusted by tuning the cut-off voltage bias of the two-stage Peak devices. The experimental results agreed well with the harmonic balance simulations using the designed amplifier with its device's non-linear models proving this technique to be an effective method of optimizing the DPA in order to meet its system requirements.

Acknowledgment

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References

[1] Lee, W., Lee, H., Kang, H., et al.: 'X-band two-stage Doherty power amplifier based on pre-matched GaN-HEMTs', IET Microwave Antenna Propagation, 2018, vol. 12, pp 179-184, 2017.

[2] Quaglia, R., Pirola, M., Ramella, C.: 'Offset lines in Doherty power amplifiers: analytical demonstration and design', IEEE Microwave Wireless Components Letters, 2013, 23, (2), pp. 93-95.

[3] Bousnina, S.: 'Analysis and design of high-efficiency variable conduction angle Doherty amplifier', IET Microwave Antennas Propagation, 2003, 3, (3), pp. 416-425.

[4] Lee, H, Kwon, J., Lim, W., et al.: 'Optimized current of the peaking amplifier for two-stage Doherty power amplifier', IEEE transactions Microwave Theory Techniques, 2017, 65, (1), pp. 209-217.

[5] Yamasaki, T., Kittaka, Y., Minamide, H., et al.: ' A 68% efficiency, C-band 100 W GaN power amplifier for space applications'. IEEE MTT-S Inst. Microwave Symp. Digest, Anaheim, CA, USA, May 2010, pp. 1384-1387.